COUNTER-BASED PHASED CLOCK GENERATOR CIRCUITS AND METHODS

ABSTRACT

Phased clock generator circuits and methods that use counters to define the desired positions of the phased output clock edges. A plurality of counters are each clocked by a count clock relatively much faster than the input clock. A first counter counts for one input clock period, and the counted value is stored. The stored value is then divided and added to provide the number of counts in various fractions of the input clock period. The divided and/or added values are provided to a second counter that counts from zero and generates various pulses at desired times throughout the input clock period. The pulses from the second counter are used (sometimes in combination with the input clock signal) to provide phased output clock signals at predetermined times during the input clock cycle. Some embodiments include a duty cycle correction feature. In some embodiments, duty cycle correction is optional.